Inventor: OGAWA et al.
Docket No.: 10873.1316US01
Title: HIGH-LEVEL SYNTHESIS METHOD

Attorney Name: Douglas P. Mueller

Phone No.: 612.371.5237

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Hardware behavioral description and design constraint

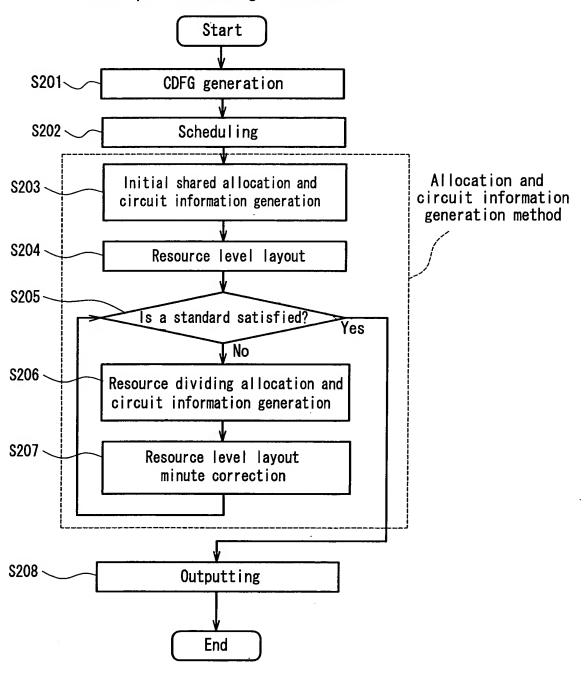


FIG. 1

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```
FUNCTION (
             unsigned int in1,
             unsigned int in2,
             unsigned int in3,
             unsigned int in4,
             unsigned int in5,
             unsigned int in6,
             unsigned int select1,
             unsigned int select2,
             unsigned int *out
             unsigned int m1, m2, m3, m4;
             m1 = in1 + in2;
             if (select1 == 0) {
                           m2 = in3 + in4;
             else {
                          m2 = in3 + in5;
             m3 = m1 + m2;
             if (select2 == 0) {
                          m4 = m3 * in6;
             } else {
                          m4 = m3 * m2;
             *out = m4;
```

FIG. 2

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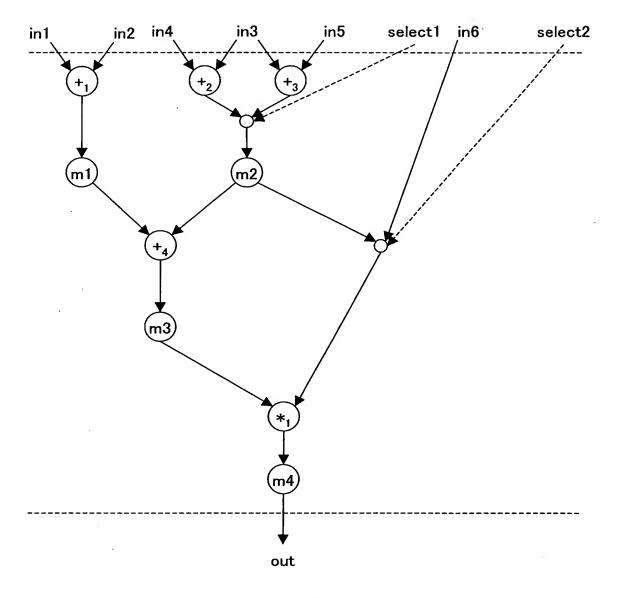


FIG. 3

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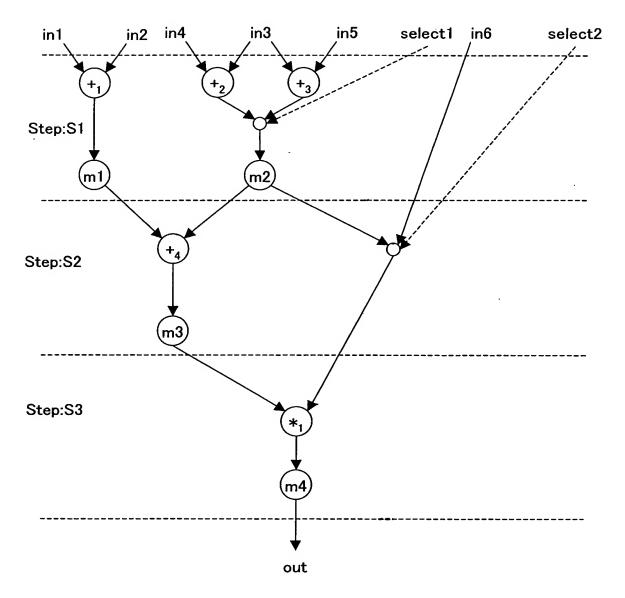


FIG. 4

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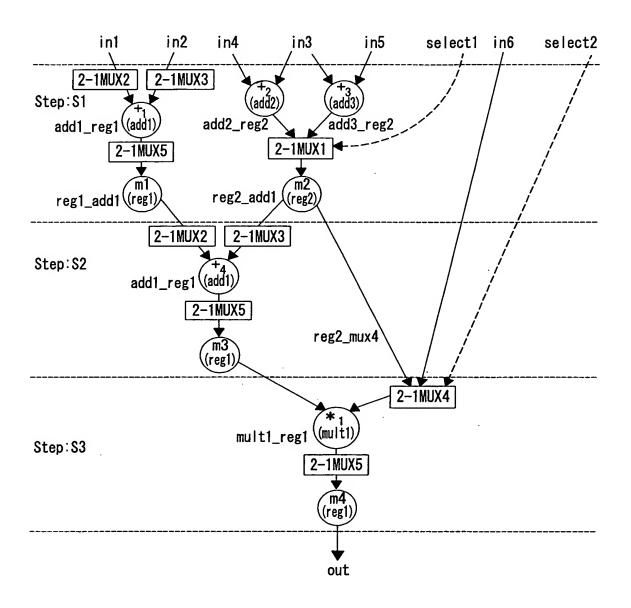
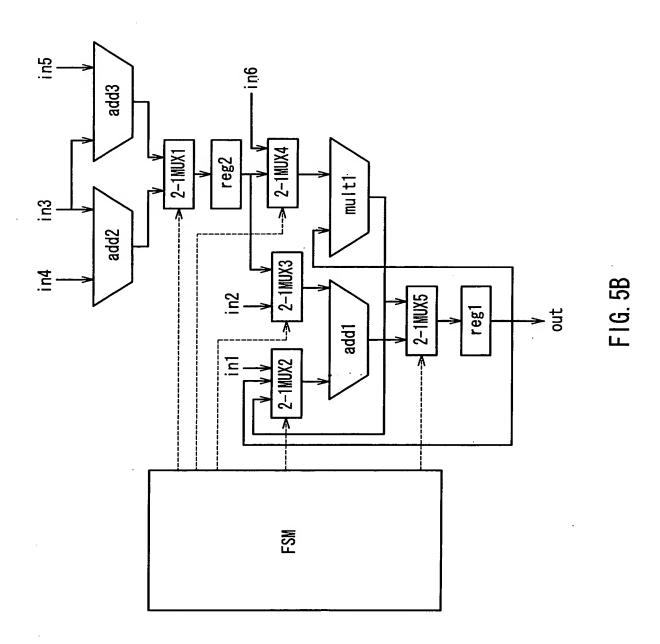


FIG. 5A

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		S1	S2	S3
	reg1	m1	m3	m4
	/ reg2 \	m2		
701	add1 \	+1	+4	
× /	add2	+2		
1	add3	+3		
	mult1			*1
	2-1MUX1	add2_reg2		•
		add3_reg2		
1	2-1MUX2	in1	reg1_add1	
	2-1MUX3	in2	reg2_add1	
,	11411			reg2_mux4
	2-1MUX4			in6
	2-1MUX5	add1_reg1	add1_reg1	mult1_reg1

FIG. 6

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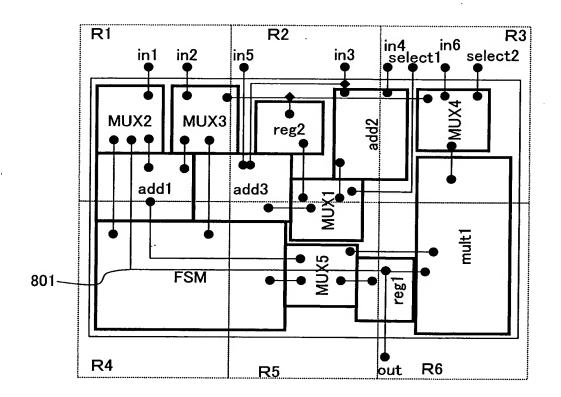


FIG. 7

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FSM	က	9	က	7	3	3	က	က	8	က	
2- 1MUX5	-	4	9	5	က	2	5	5	9		
2- 1MUX4	5	4	8	2	5	5	4	4	/		
2- 1MUX3	9	2	2	ဗ	2	4	2				
2- 1MUX2	8	က	-	4	3	5					
2- 1MUX1	3	3	4	3	2					/	
add3	2	3	2	3							
add2	ε	2	9								
add1	7	4									
reg2	. 2										
reg1											
	reg1	reg2	add1	add2	add3	2-1MUX1	2-1MUX2	2-1MUX3	2-1MUX4	2-1MUX5	FSM

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R1	R2	R3	R4	R5	R6
9	6	6	4	6	2

FIG. 9

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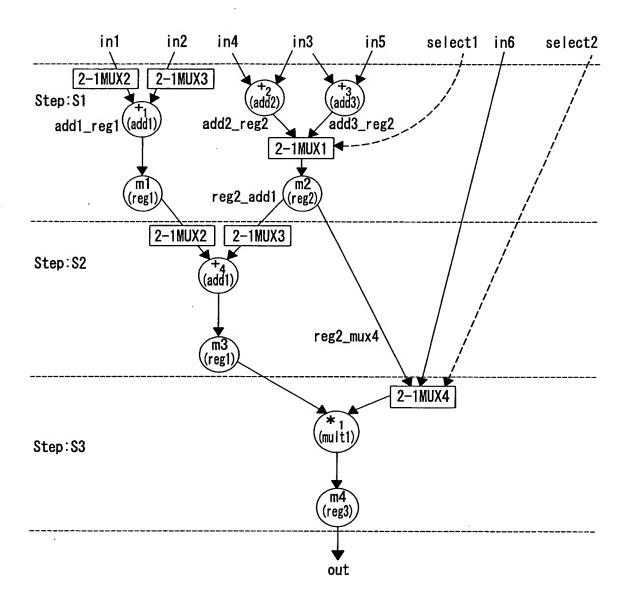
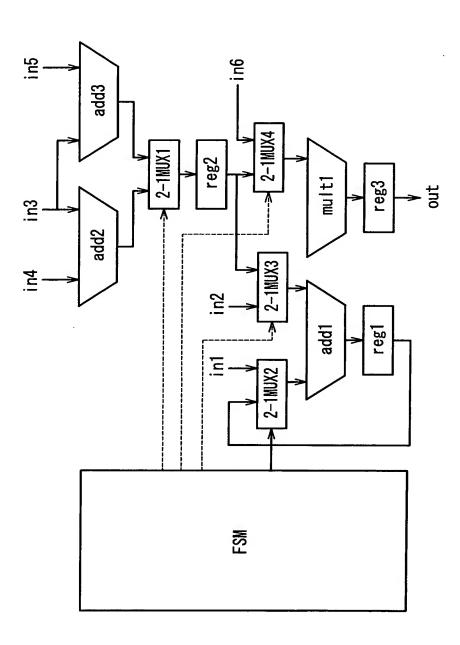


FIG. 10A

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	S1	S2	S3
reg1	m1	m3	
reg2	m2		
reg3			m4
add1	+ ₁	+4	
add2	+2		
add3	+3		
mutl1			*,
2-1MUX1	add2_reg2 add3_reg2		
2-1MUX2	in1	reg1_add1	
2-1MUX3	in2	reg2_add1	
2-1MUX4			reg2_mux4 in6

FIG. 11

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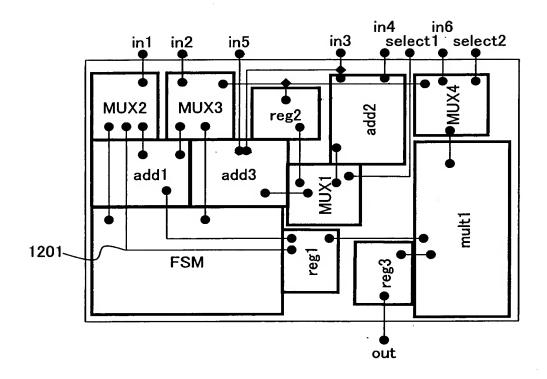


FIG. 12

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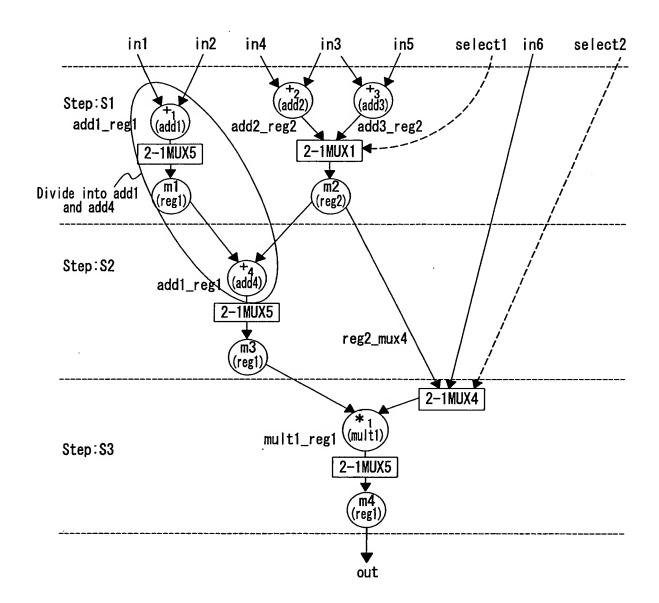
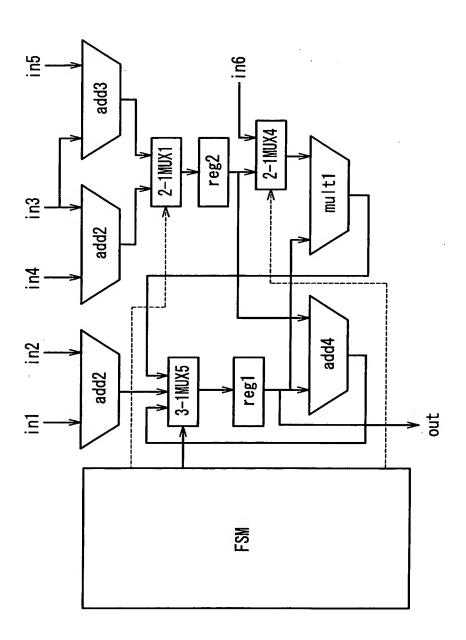


FIG. 13A

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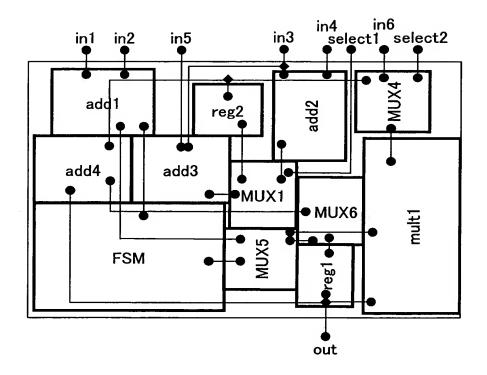


FIG. 14

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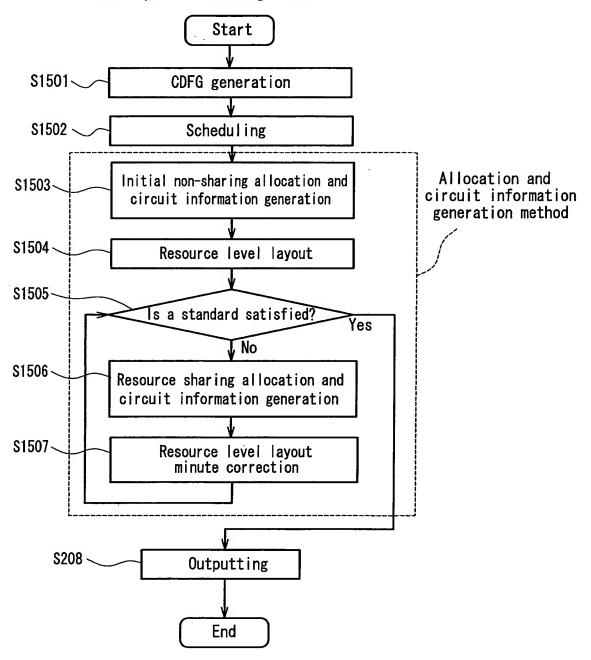


FIG. 15

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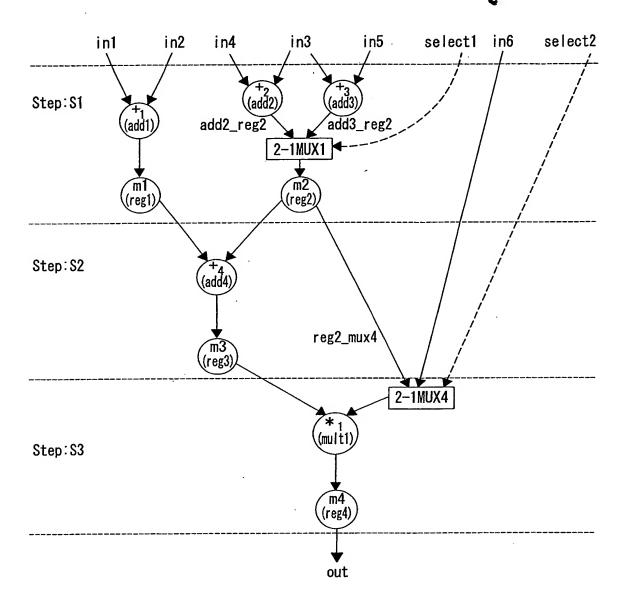
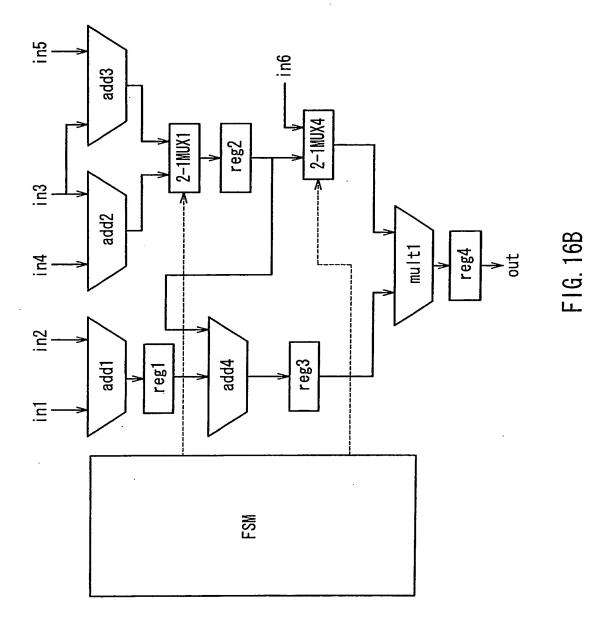


FIG. 16A

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			m2 can be shared n m3 and m4	d
	S1	S2 /	S3	
reg1	m1			
reg2	m2			
reg3		m3		
reg4			m4	
add1	+1			
add2	+2			
add3	+3			
add4		+4		
mutl1			*1	
0 11411111	add2_reg2			
2-1MUX1	add3_reg2			
2-1MUX2			reg2_mux4 in6	

FIG. 17

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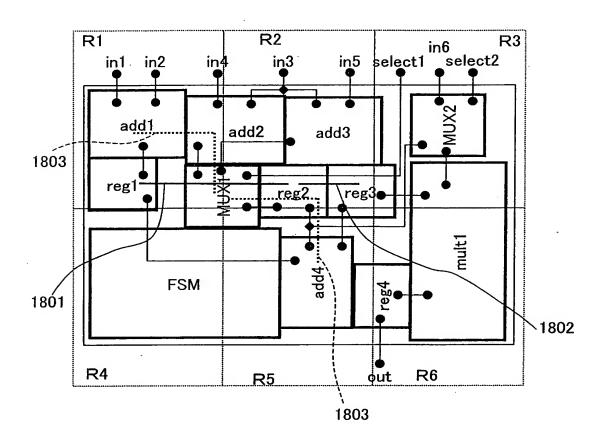


FIG. 18

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FSM	2	4	4	4	က	3	4	2	4	-	9	
2- 1MUX2	8	4	2	4	8	3	2	5	2	4		
2- 1MUX1	2	-	2	4	3	1	2	3	4			
mult1	7	က	2	-	9	5	4	2				
add4	9	4	2	_	9	4	က					
add3	2	2		က	က	_						
add2	က	2	2	4								
add1	1	2	9	6								
reg4	6	2	7									
reg3	2	1										
reg2	4											
reg1												
	reg1	reg2	reg3	reg4	add1	add2	add3	add4	mult1	2-1MUX1	2-1MUX1	FSM

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R1	R2	R3	R4	R5	R6
7	7	6	1	3	2

FIG. 20

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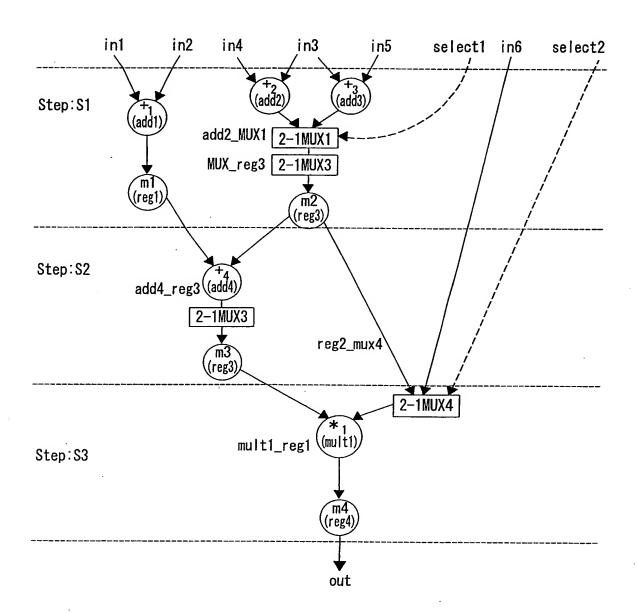
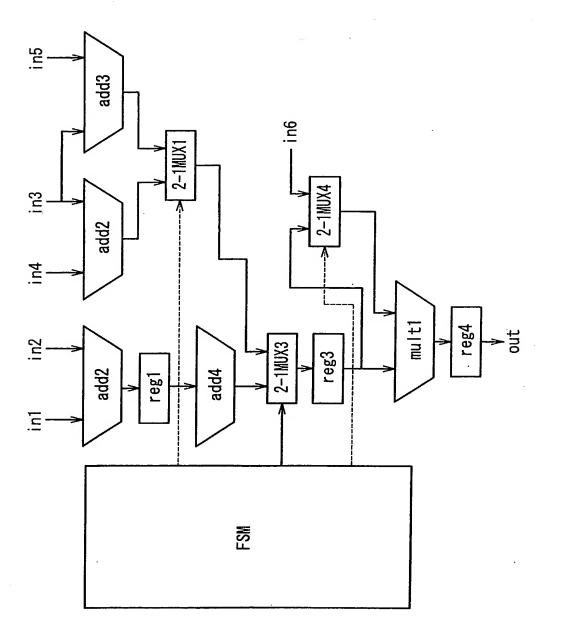


FIG. 21A

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F1G. 21B

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m2 and m3 are shared

	-		/
	S1	S2	S 3
regl	m1		
reg3	Cm2	m3	
reg4			m4
add1	+1		
add2	+2		
add3	+3		
add4		+4	
mutl1			*3
2-1MUX1	add2_reg2		
2-11/10/1	add3_reg2		
2-1MUX2			reg2_mux4
Z TIVIUAZ			in6

FIG. 22

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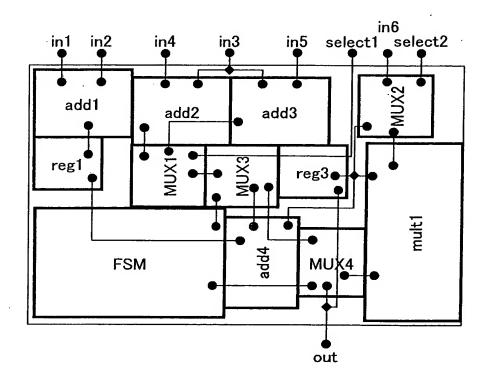


FIG. 23

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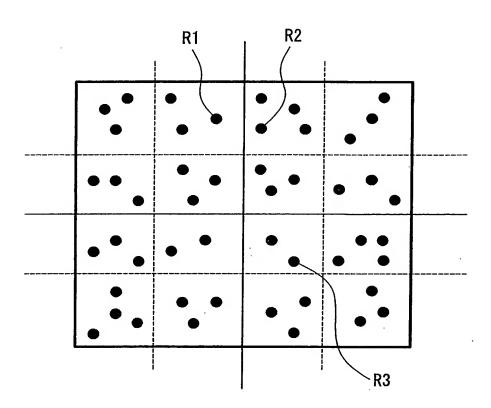


FIG. 24

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Hardware behavioral description and design constraint

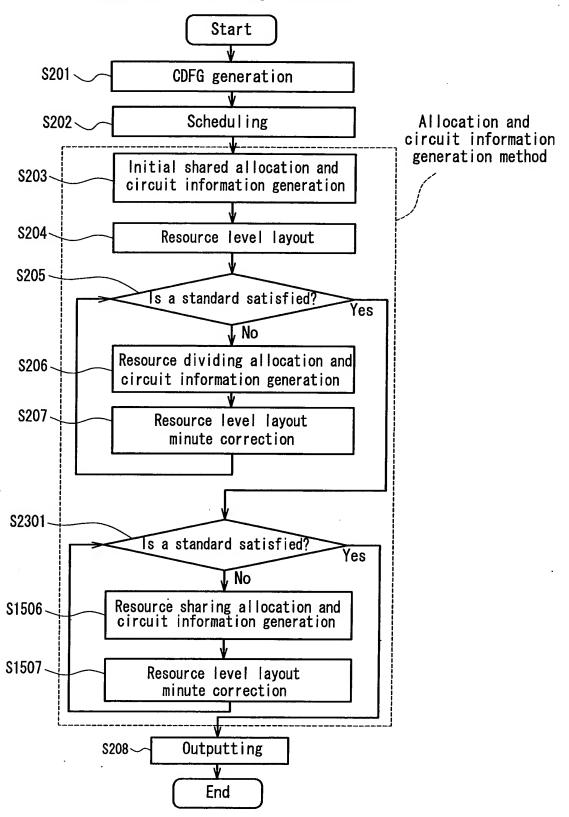


FIG. 25

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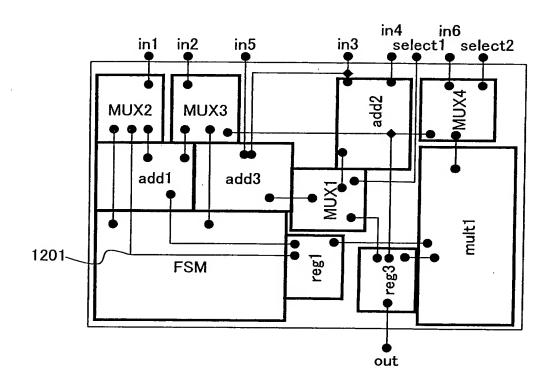


FIG. 26

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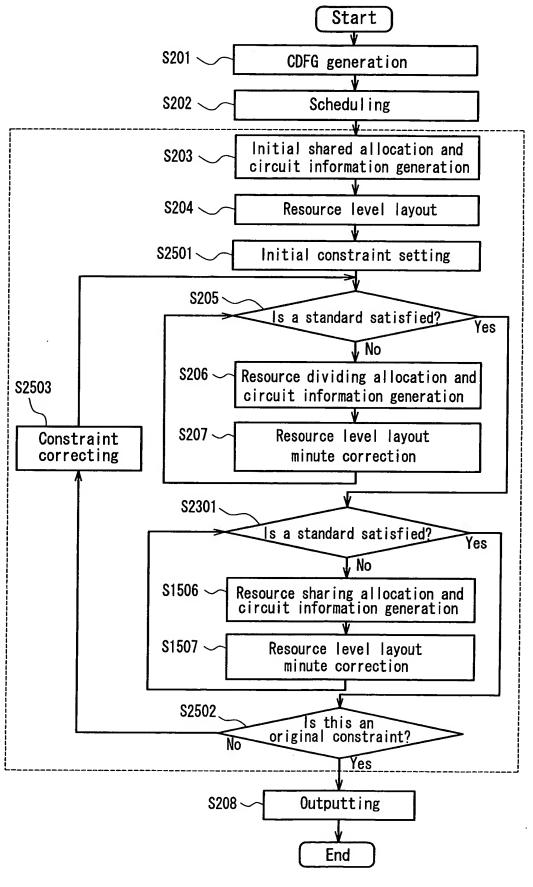


FIG. 27

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Hardware behavioral description and design constraint

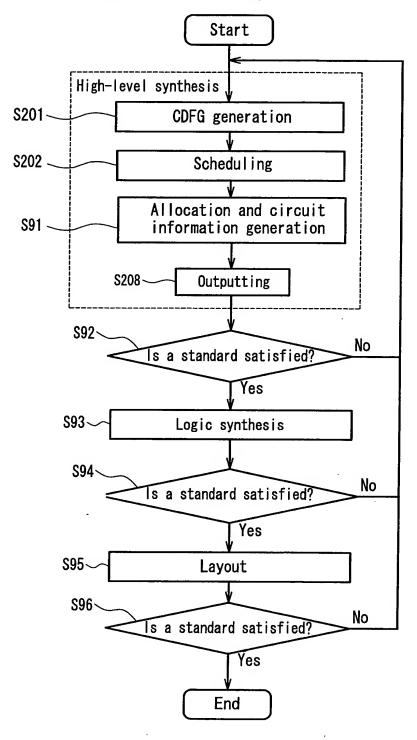


FIG. 28 PRIOR ART